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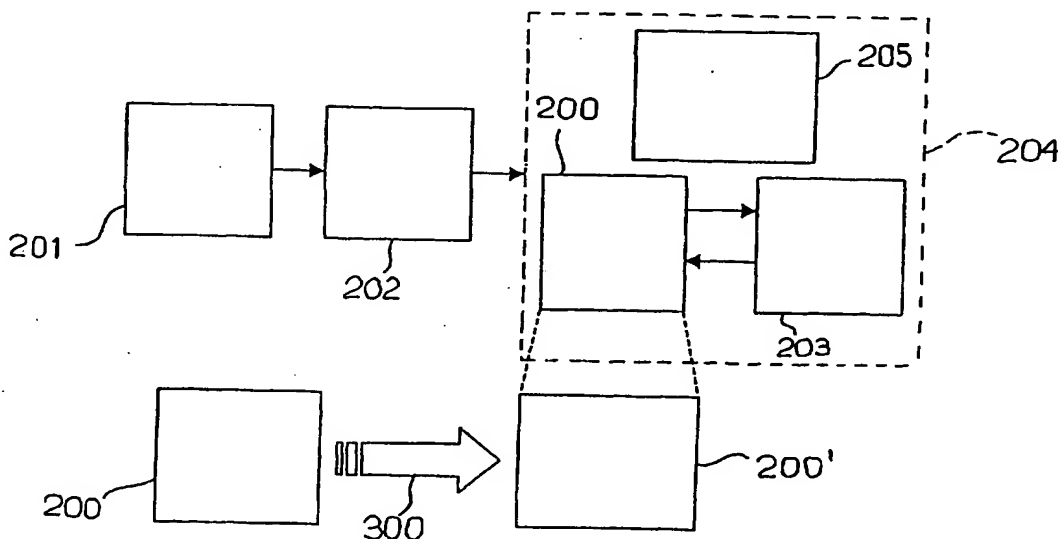
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[Continued on next page]

(54) Title: METHOD AND SYSTEM FOR VERIFYING MODULES DESTINED FOR GENERATING CIRCUITS



(57) Abstract: Models destined for verification are described at the level of synthesizable description (for example VHDL). The synthesizable description (200) is automatically converted (300) into a C++ model (200'). This allows verification of the correctness of the synthesizable description by comparing the results of a verification carried out on the original description from the cell in C++ with the results of a similar verification of the C++ model obtained by automatic conversion of the synthesizable description. It is also possible to make the C++ model obtained by automatic conversion (200') to interact with a system model including blocks (201, 202, 203) of a system model at C++ level, in particular with the possibility of producing concurrent events that occur in correspondence with a main timing signal source.



CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)
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International Application No

PCT/IT 01/00378

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 053 947 A (PARSON DALE E) 25 April 2000 (2000-04-25)	1-4
Y	column 1, line 15 - line 25 column 4, line 20 - line 50 column 12, line 50 - column 13, line 50 claim 1 figures 4-6	5
X	VAN HOOGSTRAETEN W ET AL: "ADVISE. Performance evaluation of parallel VHDL simulation" SIMULATION SYMPOSIUM, 1997. PROCEEDINGS., 30TH ANNUAL ATLANTA, GA, USA 7-9 APRIL 1997, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 7 April 1997 (1997-04-07), pages 146-156, XP010220467 ISBN: 0-8186-7934-4	1,4
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	page 4 -page 6 ----- -/--	2,3,8-15

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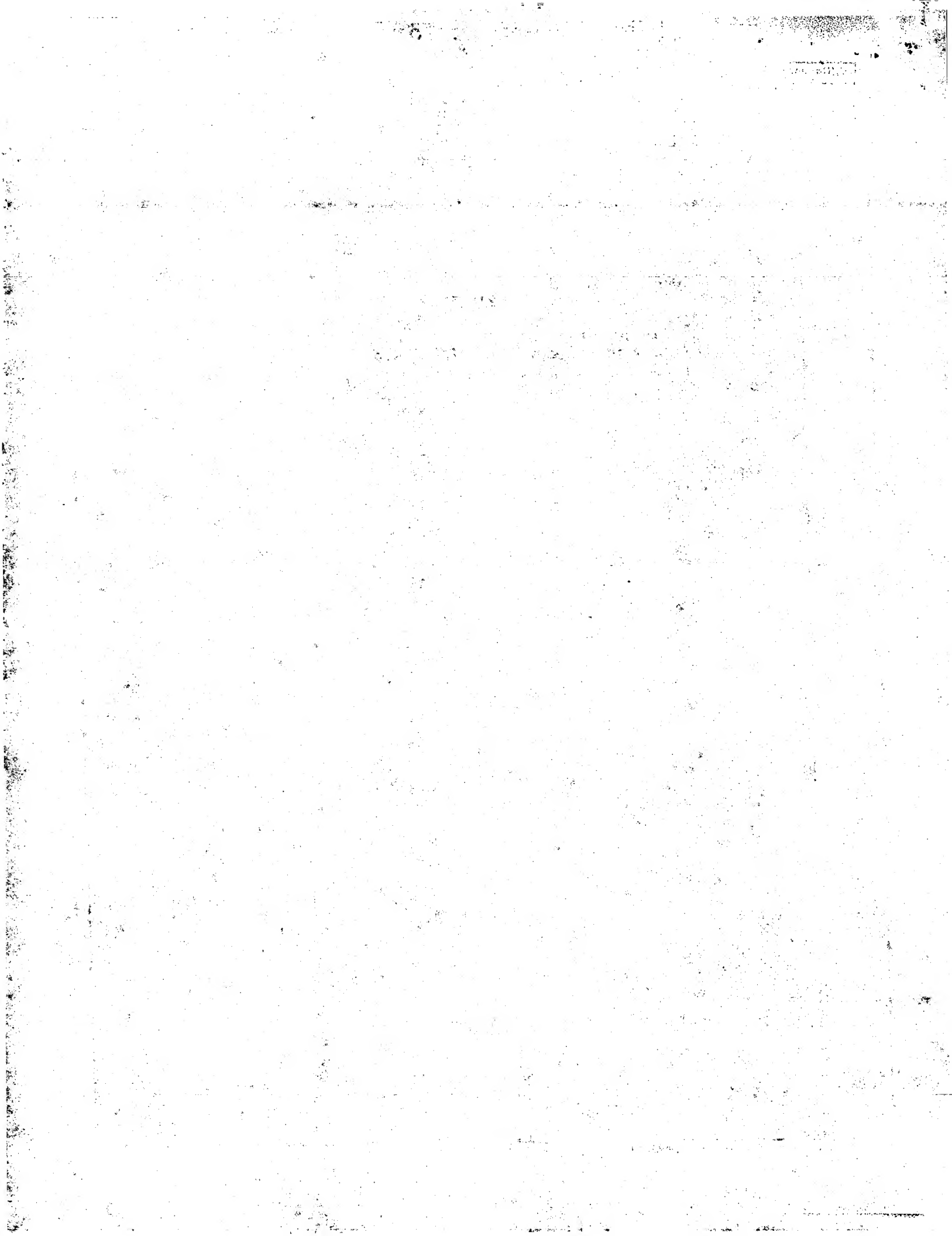
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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